

# M81720FP

HIGH VOLTAGE HALF BRIDGE DRIVER

## DESCRIPTION

M81720FP is high voltage Power MOSFET and IGBT module driver for half bridge applications.

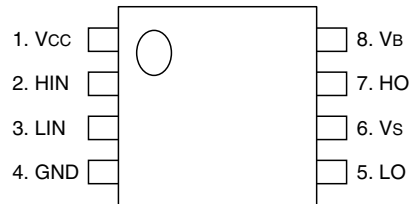
## FEATURES

- FLOATING SUPPLY VOLTAGE ..... 600V
- OUTPUT CURRENT ..... +120mA/-250mA (min)
- HALF BRIDGE DRIVER
- SOP-8 PACKAGE

## APPLICATIONS

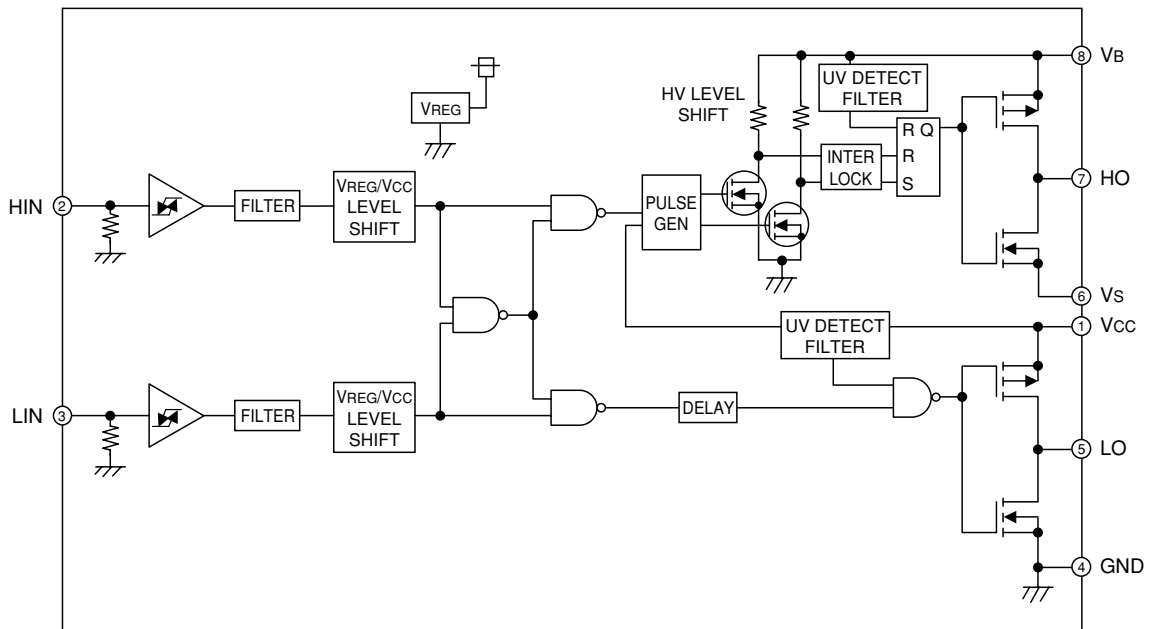
MOSFET and IGBT module inverter driver for Automotive, PDP, HID lamp, refrigerator, air-conditioner, washing machine, AC-servomotor and general purpose.

## PIN CONFIGURATION (TOP VIEW)



Outline:8P2S

## BLOCK DIAGRAM



# M81720FP

## HIGH VOLTAGE HALF BRIDGE DRIVER

### ABSOLUTE MAXIMUM RATINGS (Ta = 25°C unless otherwise specified)

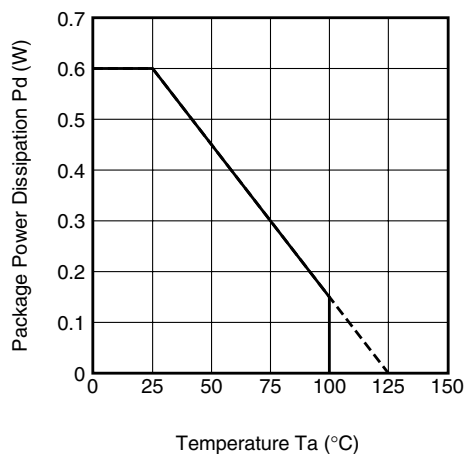
Symbol	Parameter	Test conditions	Ratings	Unit
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage		-5 ~ 600	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> = V <sub>B</sub> -V <sub>S</sub>	-0.5 ~ 24	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub> -0.5 ~ V <sub>B</sub> +0.5	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		-0.5 ~ 24	V
V <sub>LO</sub>	Low Side Output Voltage		-0.5 ~ V <sub>CC</sub> +0.5	V
V <sub>IN</sub>	Logic Input Voltage	HIN, LIN	-0.5 ~ V <sub>CC</sub> +0.5	V
P <sub>d</sub>	Package Power Dissipation	Ta = 25°C, On Board	0.6	W
K $\theta$	Linear Derating Factor	Ta > 25°C, On Board	6.0	mW/°C
R <sub>th(j-c)</sub>	Junction-Case Thermal Resistance		50	°C/W
T <sub>j</sub>	Junction Temperature		-20 ~ 125	°C
T <sub>opr</sub>	Operation Temperature		-20 ~ 100	°C
T <sub>stg</sub>	Storage Temperature		-40 ~ 125	°C

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		V <sub>S</sub> +10	—	V <sub>S</sub> +20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage		0	—	500	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> = V <sub>B</sub> -V <sub>S</sub>	10	—	20	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub>	—	V <sub>B</sub>	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		10	—	20	V
V <sub>LO</sub>	Low Side Output Voltage		0	—	V <sub>CC</sub>	V
V <sub>IN</sub>	Logic Input Voltage	HIN, LIN	0	—	7	V

\* For proper operation, the device should be used within the recommended conditions.

### THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)

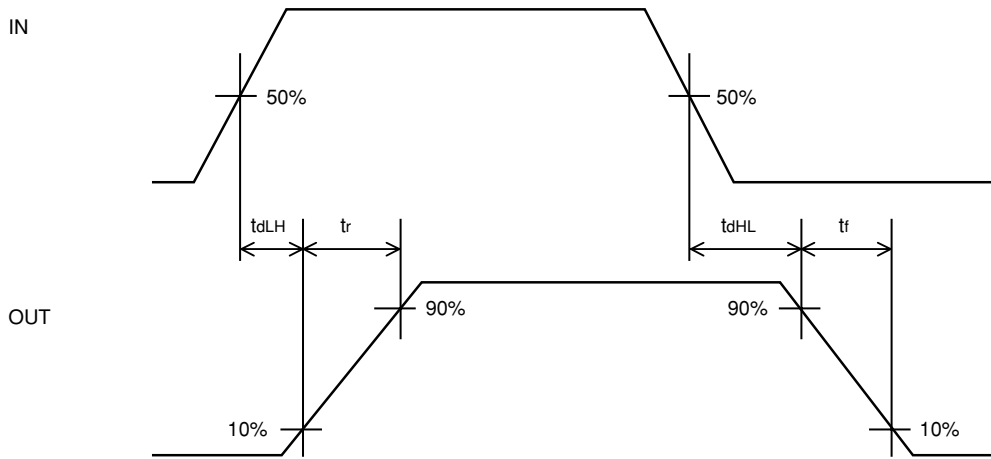


**ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vcc=Vbs(=Vb-Vs)=15V, unless otherwise specified)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
IFS	Floating Supply Leakage Current	V <sub>B</sub> = V <sub>S</sub> = 600V	—	—	1.0	μA
IBS	V <sub>BS</sub> Standby Current	HIN = LIN = 0V	—	0.2	0.5	mA
ICC	V <sub>CC</sub> Standby Current	HIN = LIN = 0V	0.2	0.6	1.0	mA
VOH	High Level Output Voltage	I <sub>O</sub> = -20mA, LO, HO	13.6	14.2	—	V
VOL	Low Level Output Voltage	I <sub>O</sub> = 20mA, LO, HO	—	0.3	0.6	V
VIH	High Level Input Threshold Voltage	HIN, LIN	2.7	—	—	V
VIL	Low Level Input Threshold Voltage	HIN, LIN	—	—	0.8	V
IiH	High Level Input Bias Current	VIN = 5V	—	5	20	μA
IiL	Low Level Input Bias Current	VIN = 0V	—	—	2	μA
VBSuvr	V <sub>BS</sub> Supply UV Reset Voltage		8.0	8.9	9.8	V
VBSuvt	V <sub>BS</sub> Supply UV Trip Voltage		7.4	8.2	9.0	V
VBSuvh	V <sub>BS</sub> Supply UV Hysteresis Voltage		0.5	0.7	—	V
tVBSuv	V <sub>BS</sub> Supply UV Filter Time		—	7.5	—	μs
VCCuvr	V <sub>CC</sub> Supply UV Reset Voltage		8.0	8.9	9.8	V
VCCuvt	V <sub>CC</sub> Supply UV Trip Voltage		7.4	8.2	9.0	V
VCCuvh	V <sub>CC</sub> Supply UV Hysteresis Voltage		0.5	0.7	—	V
tVCCuv	V <sub>CC</sub> Supply UV Filter Time		—	7.5	—	μs
IOH	Output High Level Short Circuit Pulsed Current	V <sub>O</sub> = 0V, V <sub>IN</sub> = 5V, PW < 10μs	120	200	—	mA
IOL	Output Low Level Short Circuit Pulsed Current	V <sub>O</sub> = 15V, V <sub>IN</sub> = 0V, PW < 10μs	250	350	—	mA
ROH	Output High Level On Resistance	I <sub>O</sub> = -20mA, R <sub>OH</sub> = (V <sub>CC</sub> -V <sub>O</sub> )/I <sub>O</sub>	—	40	70	Ω
ROL	Output Low Level On Resistance	I <sub>O</sub> = 20mA, R <sub>OL</sub> = V <sub>O</sub> /I <sub>O</sub>	—	15	30	Ω
tdLH(HO)	High Side Turn-On Propagation Delay	CL = 1000pF between HO-Vs	—	450	650	ns
tdHL(HO)	High Side Turn-Off Propagation Delay	CL = 1000pF between HO-Vs	—	450	650	ns
trH	High Side Turn-On Rise Time	CL = 1000pF between HO-Vs	—	130	220	ns
tfH	High Side Turn-Off Fall Time	CL = 1000pF between HO-Vs	—	50	80	ns
tdLH(LO)	Low Side Turn-On Propagation Delay	CL = 1000pF between LO-GND	—	450	650	ns
tdHL(LO)	Low Side Turn-Off Propagation Delay	CL = 1000pF between LO-GND	—	450	650	ns
trL	Low Side Turn-On Rise Time	CL = 1000pF between LO-GND	—	130	220	ns
tfL	Low Side Turn-Off Fall Time	CL = 1000pF between LO-GND	—	50	80	ns
ΔtdLH	Delay Matching, High Side and Low Side Turn-On	tdLH(HO)-tdLH(LO)	—	0	30	ns
ΔtdHL	Delay Matching, High Side and Low Side Turn-Off	tdHL(HO)-tdHL(LO)	—	0	30	ns
Tinon	Input Filter Time (ON)	CONVEX PULSE	150	250	350	ns
		CONCAVE PULSE	250	350	450	ns
Tinoff	Input Filter Time (OFF)	CONVEX PULSE	150	250	350	ns
		CONCAVE PULSE	250	350	450	ns
ΔPWIO	I/O Pulse Width Difference	PW(IN)-PW(OUT)	-40	0	100	ns

\* Typ. is not specified.

**TIMING REQUIREMENT (Input Signal Frequency : 200kHz Duty < 50%)**



**FUNCTION TABLE**

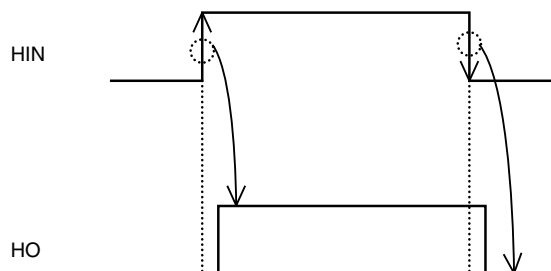
HIN	LIN	Vbs UV	Vcc UV	HO	LO	Behavioral state
H→L	L	H	H	L	L	LO = HO = Low
H→L	H	H	H	L	H	LO = High
L→H	L	H	H	H	L	HO = High
L→H	H	H	H	L	L	LO = HO = Low
X	L	L	H	L	L	HO = Low, Vbs UV tripped
X	H	L	H	L	H	LO = High, Vbs UV tripped
H→L	X	H	L	L	L	LO = Low, Vcc UV tripped
L→H	X	H	L	L	L	HO = LO = Low, Vcc UV tripped

Note1 : "L" state of Vbs UV, Vcc UV means that UV trip voltage.

2 : In the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) become "L".

3 : X (HIN) : L→H or H→L. X(LIN) : H or L.

4 : Output signal (HO) is triggered by the edge of input signal.

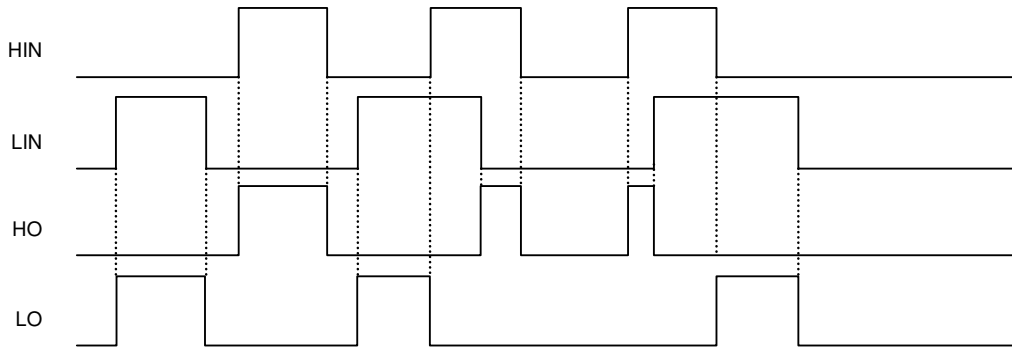


**TIMING DIAGRAM**

1. Input/Output Timing Diagram

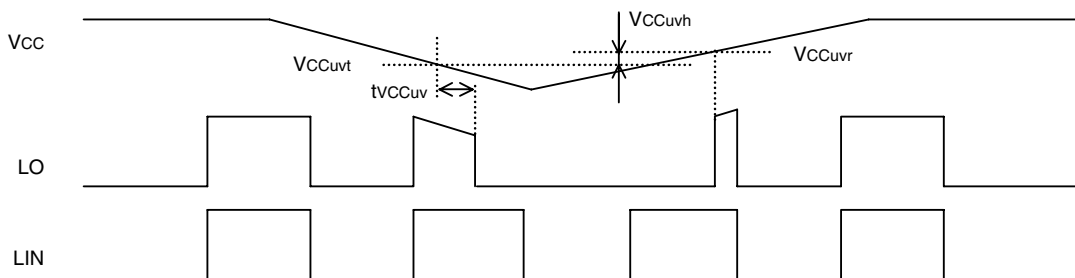
HIGH ACTIVE (When input signal (HIN or LIN) is "H", then output signal (HO or LO) is "H".)

In the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) become "L".

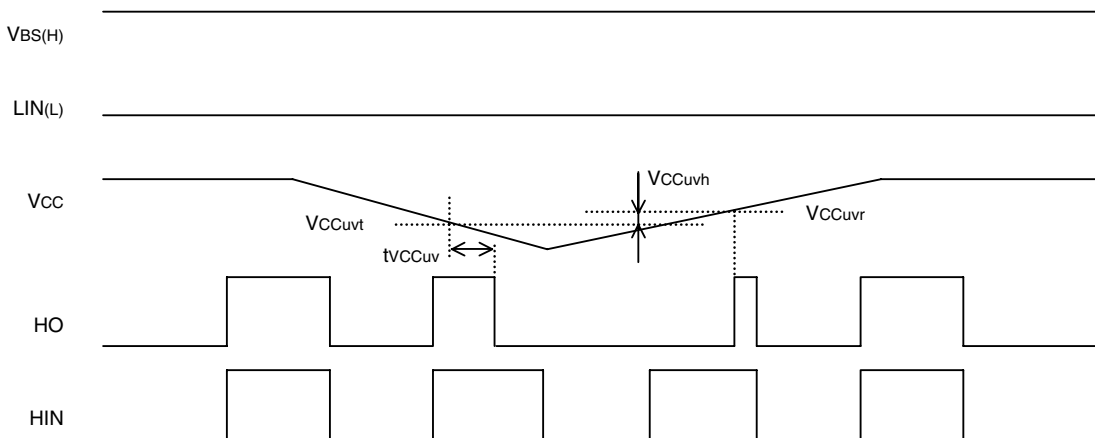


2. Vcc (Vbs) Supply Under Voltage Lockout Timing Diagram

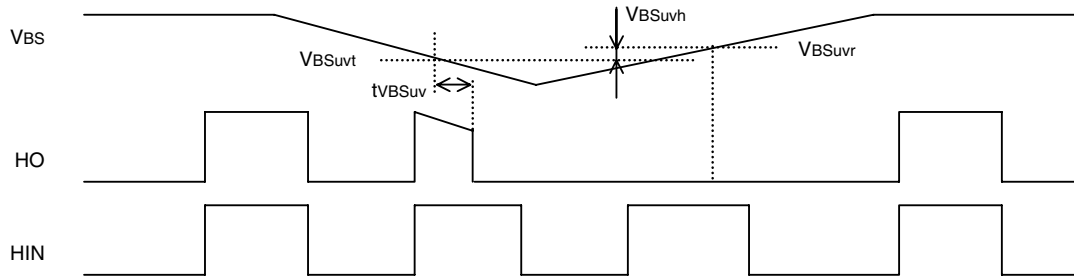
If Vcc supply voltage drops below UV trip voltage ( $V_{CCuvl}$ ) for Vcc Supply UV filter time, output signal is shut down. As soon as Vcc supply voltage rises over UV reset voltage, output signal LO becomes "H" if LIN is "H".



If Vcc supply voltage drops below UV trip voltage ( $V_{CCuvl}$ ) for Vcc supply UV filter time, output signal is shut down. As soon as Vcc supply voltage rises over UV reset voltage, output signal HO becomes "H" if HIN is "H".



If VBS supply voltage drops below UV trip voltage ( $V_{BSuvt}$ ) for VBS supply UV filter time, output signal is shut down. As soon as VBS supply voltage rises over UV reset voltage, output signal HO becomes "H" at following "H" HIN input signal.



3. Allowable Supply Voltage Transient

It is recommended to supply VCC firstly and supply VBS secondly. In the case of shutting off supply voltage, please shut off VBS firstly and shut off VCC secondly. When applying VCC and VBS, power supply should be applied slowly. If it rises rapidly, output signal (HO or LO) may be malfunction.

4. About the deadtime between HIN and LIN.

Due to input filter circuit, the pulse width of output maybe longer than the pulse width of input. In that case, please assure that the deadtime between HIN and LIN is over 300ns, or HO and LO maybe on at the same time (shut-through).

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## HIGH VOLTAGE HALF BRIDGE DRIVER

### Consideration

As for this product, the terminal of low voltage part and high-voltage part is very clear (The Fifth: LO, The Sixth: Vs). Therefore, pin insulation space distance should be taken enough.

### PACKAGE OUTLINE

