

# M81722FP

## HIGH VOLTAGE HALF BRIDGE DRIVER

### DESCRIPTION

M81722FP is high voltage Power MOSFET and IGBT driver for half bridge applications.

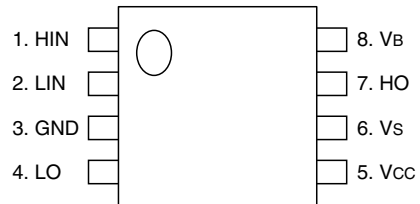
### FEATURES

- FLOATING SUPPLY VOLTAGE ..... 600V
- OUTPUT CURRENT ..... ±3A (typ)
- UNDERVOLTAGE LOCKOUT
- INPUT FILTER
- SOP-8 PACKAGE

### APPLICATIONS

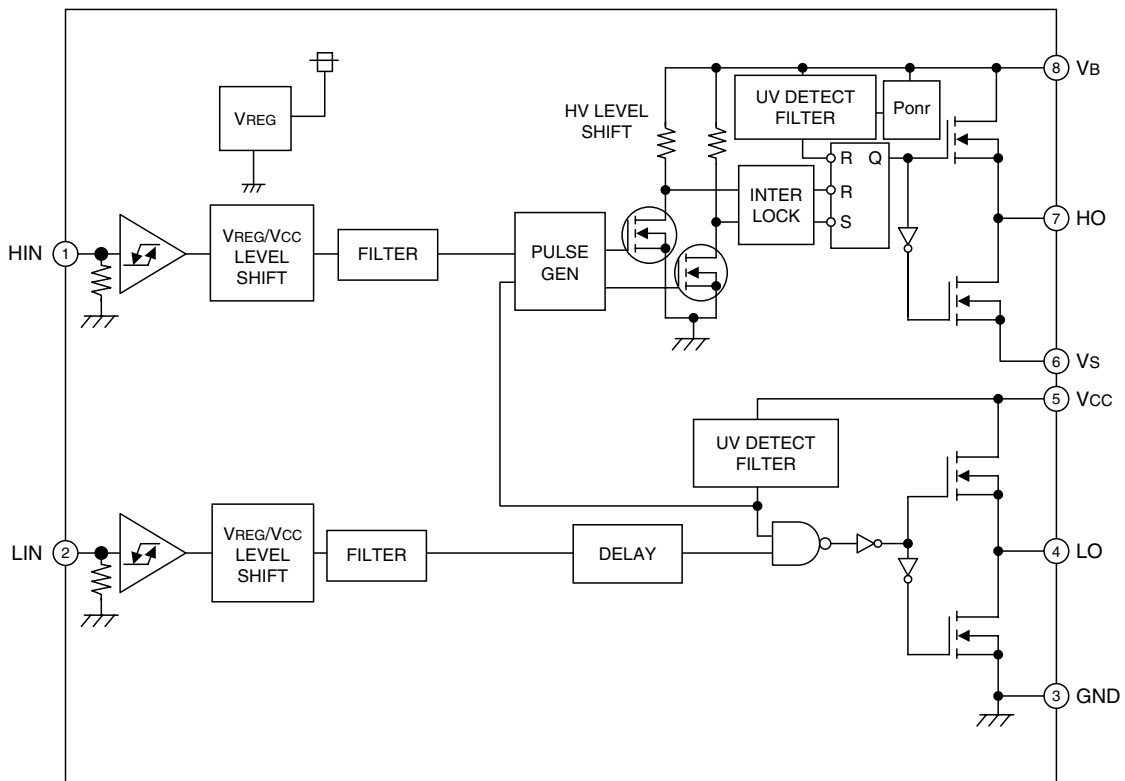
MOSFET and IGBT driver for PDP,HID lamp, refrigerator, air-conditioner, washing machine, AC-servomotor and general purpose.

### PIN CONFIGURATION (TOP VIEW)



Outline:8P2S

### BLOCK DIAGRAM



# M81722FP

## HIGH VOLTAGE HALF BRIDGE DRIVER

### ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Ratings	Unit
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage		V <sub>B</sub> -24 ~ V <sub>B</sub> +0.5	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> = V <sub>B</sub> -V <sub>S</sub>	-0.5 ~ 24	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub> -0.5 ~ V <sub>B</sub> +0.5	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		-0.5 ~ 24	V
V <sub>LO</sub>	Low Side Output Voltage		-0.5 ~ V <sub>CC</sub> +0.5	V
V <sub>IN</sub>	Logic Input Voltage	HIN, LIN	-0.5 ~ V <sub>CC</sub> +0.5	V
P <sub>d</sub>	Package Power Dissipation	Ta = 25°C , On Board	0.6	W
K $\theta$	Linear Derating Factor	Ta > 25°C , On Board	4.8	mW/°C
R <sub>th(j-c)</sub>	Junction - Case Thermal Resistance		50	°C/W
T <sub>j</sub>	Junction Temperature		-20 ~ 150*	°C
T <sub>opr</sub>	Operation Temperature		-20 ~ 125	°C
T <sub>stg</sub>	Storage Temperature		-40 ~ 150	°C
TL	Solder heat-proof(flow)	For RoHS	260 (10s)	°C

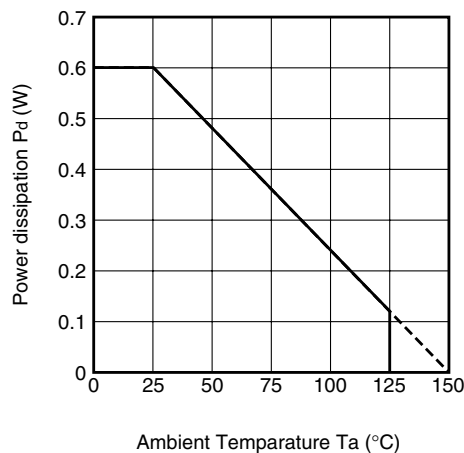
\* Please adjust the V<sub>S</sub> potential to 500V or less when the junction temperature (T<sub>j</sub>) exceeds 125°C.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage		V <sub>S</sub> +10	—	V <sub>S</sub> +20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> > 10V	-5	—	500	V
V <sub>BS</sub>	High Side Floating Supply Voltage	V <sub>BS</sub> = V <sub>B</sub> -V <sub>S</sub>	10	—	20	V
V <sub>HO</sub>	High Side Output Voltage		V <sub>S</sub>	—	V <sub>B</sub>	V
V <sub>CC</sub>	Low Side Fixed Supply Voltage		10	—	20	V
V <sub>LO</sub>	Logic Supply Voltage		0	—	V <sub>CC</sub>	V
V <sub>IN</sub>	Logic Input Voltage	HIN, LIN	0	—	7	V

\* For proper operation, the device should be used within the recommended conditions.

### THERMAL DERATING FACTOR CHARACTERISTIC (ABSOLUTE MAXIMUM RATINGS)

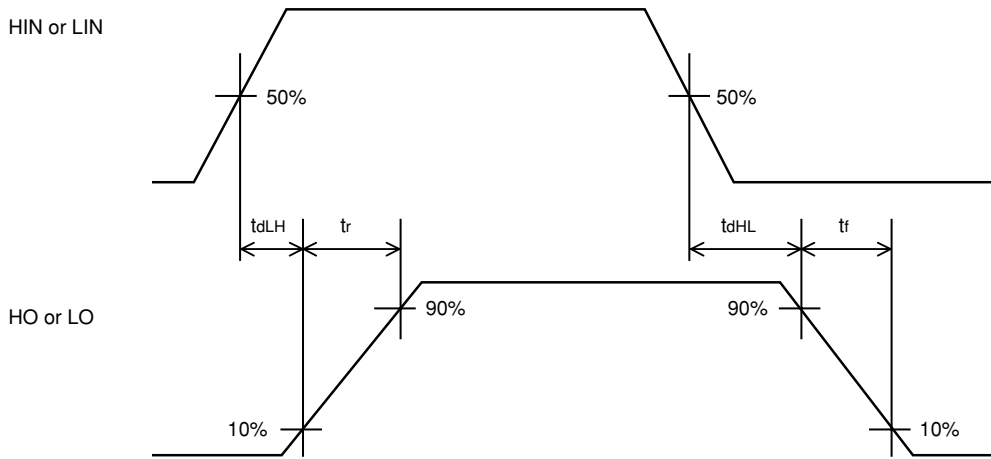


**ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vcc=Vbs(=Vb-Vs)=15V, unless otherwise specified)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
IFS	Floating Supply Leakage Current	V <sub>B</sub> = V <sub>S</sub> = 600V	—	—	1.0	μA
IBS	VBS standby Current	HIN = LIN = 0V	—	0.2	0.5	mA
ICC	Vcc standby Current	HIN = LIN = 0V	—	0.6	1.0	mA
VOH	High Level Output Voltage	I <sub>O</sub> = 0A, LO, HO	13.8	14.4	—	V
VOL	Low Level Output Voltage	I <sub>O</sub> = 0A, LO, HO	—	—	0.1	V
VIH	High Level Input Threshold Voltage	HIN, LIN	4.0	—	—	V
VIL	Low Level Input Threshold Voltage	HIN, LIN	—	—	0.8	V
IiH	High Level Input Bias Current	V <sub>IN</sub> = 5V	—	17	40	μA
IiL	Low Level Input Bias Current	V <sub>IN</sub> = 0V	—	—	1	μA
VBSuvr	VBS Supply UV Reset Voltage		8.0	8.9	9.8	V
VBSuvh	VBS Supply UV Hysteresis Voltage		0.3	0.7	—	V
tVBSuv	VBS Supply UV Filter Time		—	7.5	—	μs
VCCuvr	Vcc Supply UV Reset Voltage		8.0	8.9	9.8	V
VCCuvh	Vcc Supply UV Hysteresis Voltage		0.3	0.7	—	V
tVCCuv	Vcc Supply UV Filter Time		—	7.5	—	μs
VPonr	Power-On Reset Voltage		—	—	6.0**	V
tPonr(FIL)	Power-On Reset Filter Time		300**	—	—	ns
IOH	Output High Level Short Circuit Pulsed Current	V <sub>O</sub> = 0V, V <sub>IN</sub> = 5V, PWD < 10μs	2.0	3.0	—	A
IOL	Output Low Level Short Circuit Pulsed Current	V <sub>O</sub> = 15V, V <sub>IN</sub> = 0V, PWD < 10μs	2.0	3.0	—	A
ROH	Output High Level On Resistance	I <sub>O</sub> = -200mA, R <sub>OH</sub> = (V <sub>OH</sub> -V <sub>O</sub> ) / I <sub>O</sub>	—	10	20	Ω
ROL	Output Low Level On Resistance	I <sub>O</sub> = 200mA, R <sub>OL</sub> = V <sub>O</sub> / I <sub>O</sub>	—	2.5	3.0	Ω
tdLH(HO)	High Side Turn-On Propagation Delay	CL = 1000pF between HO-Vs	—	200	280	ns
tdHL(HO)	High Side Turn-Off Propagation Delay	CL = 1000pF between HO-Vs	—	180	260	ns
trH	High Side Turn-On Rise Time	CL = 1000pF between HO-Vs	—	25	45	ns
tfH	High Side Turn-Off Fall Time	CL = 1000pF between HO-Vs	—	20	35	ns
tdLH(LO)	Low Side Turn-On Propagation Delay	CL = 1000pF between LO-GND	—	200	280	ns
tdHL(LO)	Low Side Turn-Off Propagation Delay	CL = 1000pF between LO-GND	—	180	260	ns
trL	Low Side Turn-On Rise Time	CL = 1000pF between LO-GND	—	25	45	ns
tfL	Low Side Turn-Off Fall Time	CL = 1000pF between LO-GND	—	20	35	ns
ΔtdLH	Delay Matching, High Side and Low Side Turn-On	tdLH (HO) -tdLH (LO)	—	0	30	ns
ΔtdHL	Delay Matching, High Side and Low Side Turn-Off	tdHL (HO) -tdHL (LO)	—	0	30	ns
IN(FIL)	Input Filter Time	CONVEX PULSE : HIN, LIN	—	100	—	ns
		CONCAVE PULSE : HIN, LIN	—	100	—	ns

\* Typ. is not specified  
 \*\* High Side Circuit Only

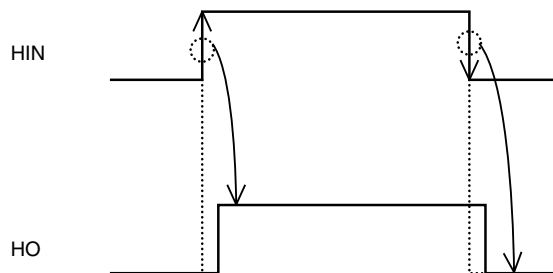
**TIMING REQUIREMENT**



**FUNCTION TABLE**

HIN	LIN	V <sub>BS</sub> UV	V <sub>CC</sub> UV	HO	LO	Behavioral state
H→L	L	H	H	L	L	LO = HO = Low
H→L	H	H	H	L	H	LO = High
L→H	L	H	H	H	L	HO = High
L→H	H	H	H	H	H	LO = HO = High
X	L	L	H	L	L	HO = Low, V <sub>BS</sub> UV tripped
X	H	L	H	L	H	LO = High, V <sub>BS</sub> UV tripped
H→L	X	H	L	L	L	LO = Low, V <sub>CC</sub> UV tripped
L→H	X	H	L	L	L	HO = LO = Low, V <sub>CC</sub> UV tripped

- Note1 : "L" state of V<sub>BS</sub> UV, V<sub>CC</sub> UV means that UV trip voltage.  
 2 : When input signal (HIN and LIN) is "H" at the same time, then output signal (Both HO and LO) is "H".  
 3 : X(HIN) : L→H or H→L, X(LIN) : H or L.  
 4 : Output signal (HO) is triggered by the edge of input signal.

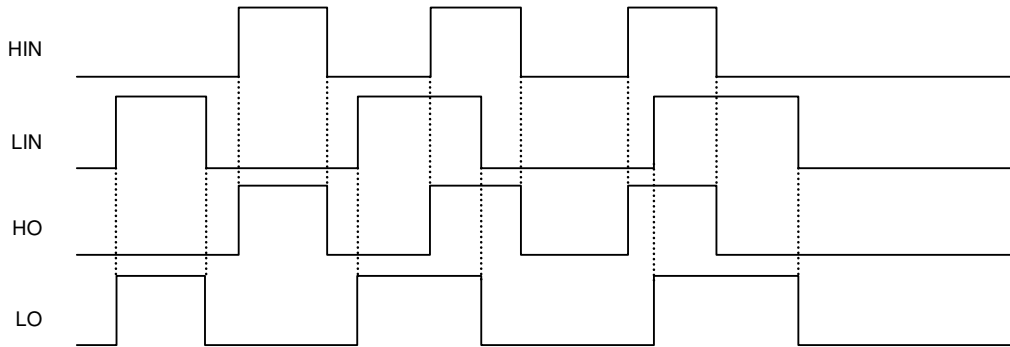


**TIMING DIAGRAM**

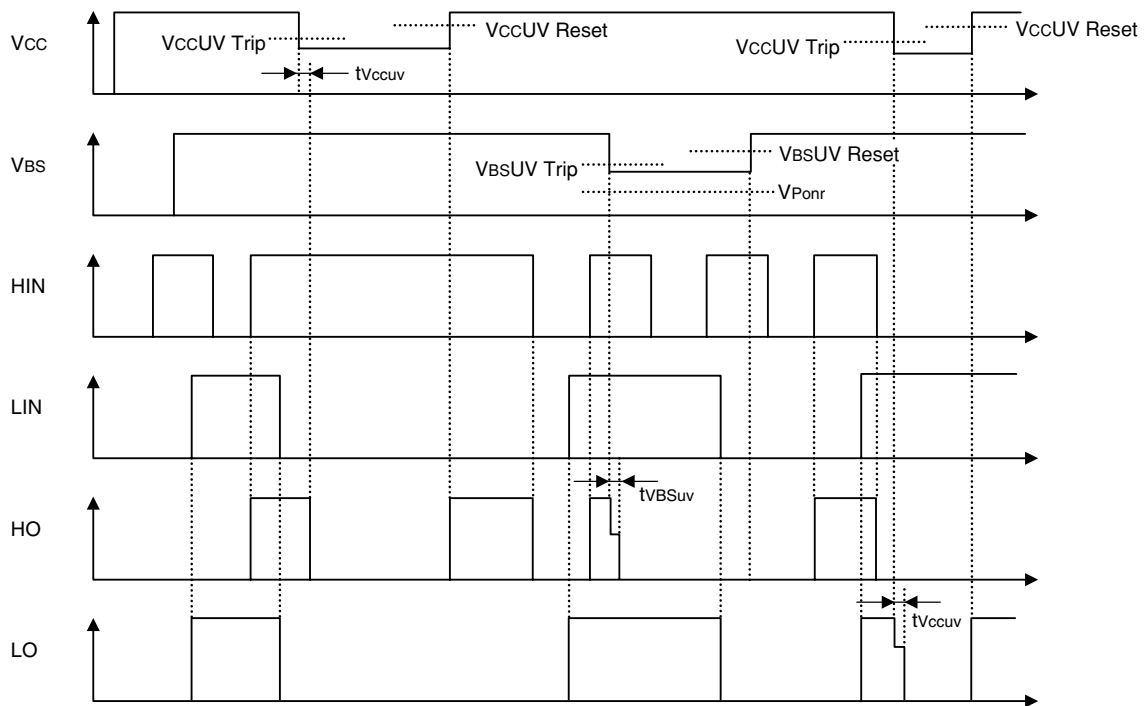
1. Input/Output Timing Diagram

HIGH ACTIVE (When input signal (HIN or LIN) is "H", then output signal (HO or LO) is "H".)

Because there is not interlock circuit, in the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) become "H".



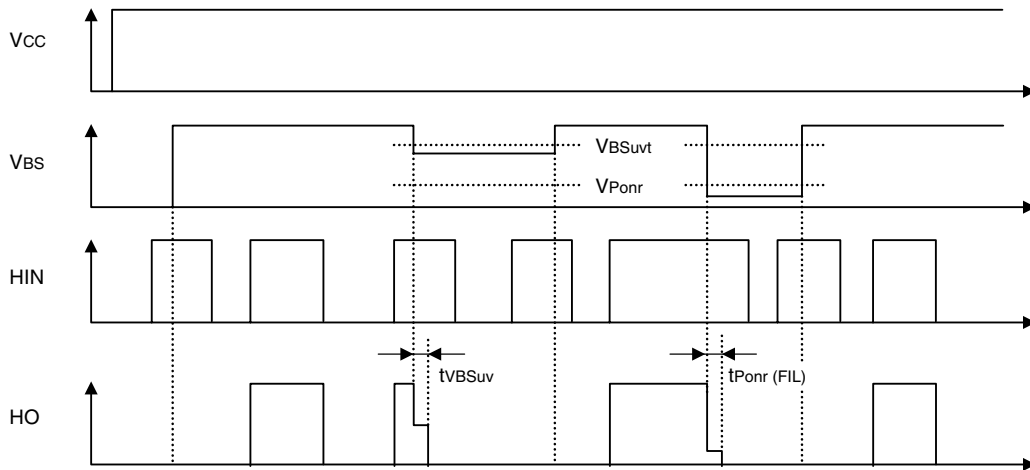
2. Operation sequence Diagram



• Logic During UV Error

Error Signal	HO	LO
UV Error (Vcc)	HO is locked at "L" Level during Vcc UV error is detected. HO responds to HIN ,if Vcc exceeds Vcc UV reset level.	LO is locked at "L" Level during Vcc UV error is detected. LO responds to LIN ,if Vcc exceeds Vcc UV reset level.
UV Error (Vbs)	HO is locked at "L" Level during Vcc UV error is detected. After Vbs exceeds Vbs UV reset level, the undervoltage lockout of HO is removed by "L"input signal of HIN,and then HO responds to the input signal.	LO responds to LIN even if Vbs voltage is UV error.

3. Ponr sequence Diagram



\* When supply voltage is lower than VPonr, then output will go low after tPonr(FIL).

4. Allowable supply voltage transient

It is recommended to supply Vcc firstly and supply Vbs secondly. In the case of shutting off supply voltage, please shut off Vbs firstly and shut off Vcc secondly. When applying Vcc and Vbs, power supply should be applied slowly. If it rises rapidly, output signal (HO or LO) may be malfunction.

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## HIGH VOLTAGE HALF BRIDGE DRIVER

### Consideration

As for this product, the terminal of low voltage part and high-voltage part is very clear (The Fifth: Vcc, The Sixth: Vs). Therefore, pin insulation space distance should be taken enough.

### PACKAGE OUTLINE

